

WE CLAIM:

1. A structure for the protection of functional circuitry from electrostatic discharge at a terminal, comprising:

a pump transistor disposed at a semiconducting surface of a substrate of a first conductivity type, comprising:

5 a drain region of a second conductivity type, connected to the terminal and disposed within a well region of the second conductivity type at the surface;

a gate electrode, overlapping a portion of the well region within which the drain region is disposed, and insulated from a channel region by a gate dielectric, the channel region being of the first conductivity type; and

10 a source region, disposed at the surface adjacent to the channel region;

a protection transistor disposed at the surface of the substrate, comprising:

a drain region connected to the drain region of the pump transistor;

a source region; and

a gate electrode connected to the gate electrode of the pump transistor

15 and insulatively disposed over a channel region of the substrate located between the source region and the drain region; and

a guard ring of the first conductivity type surrounding the protection transistor, and connected to the source region of the pump transistor.

2. The structure of claim 1, wherein the drain region of the protection transistor is also disposed within a well region of the second conductivity type at the surface.

3. The structure of claim 1, wherein each of the source and drain regions of the pump and protection transistors are clad with a metal silicide film.

4. The structure of claim 1, further comprising:

a junction capacitor, having a first plate connected to the drain regions of the pump and protection transistors and to the terminal, and having a second plate connected to the gate electrodes of the pump and protection transistors.

5. The structure of claim 1, further comprising:

a junction diode, having an anode connected to the terminal and to the drain region of the pump transistor, and having a cathode connected to a power supply node.

6. The structure of claim 5, wherein the junction diode comprises:

a diffused anode region of the first conductivity type disposed within a well of the second conductivity type, and connected to the terminal and to the drain region of the pump transistor;

5 a diffused cathode region of the second conductivity type disposed within the well of the second conductivity type, and connected to the power supply node.

7. The structure of claim 1, further comprising:

a control circuit, connected to the gates of the pump and protection transistors, and coupled to a power supply node, for biasing the gates of the pump and protection transistors to an off state responsive to the power supply node receiving a 5 power supply voltage.

8. The structure of claim 1, wherein the protection transistor is arranged as a plurality of individual protection transistors connected in parallel;

wherein the pump transistor is arranged as a plurality of individual pump transistors connected in parallel;

5 wherein the plurality of individual pump transistors and the plurality of individual protection transistors are arranged in a plurality of blocks;

and wherein each of the plurality of blocks is surrounded by a portion of the guard ring.

9. The structure of claim 1, wherein the pump transistor has an effective channel length that is shorter than that of the protection transistor.

10. A method of conducting current applied to a terminal of an integrated circuit by an electrostatic discharge event, comprising:

conducting the current to a drain of a pump transistor;

capacitively coupling the current from the drain of the pump transistor to

5 a gate of the pump transistor, the gate overlapping a portion of a well within which the drain is disposed to define the capacitance, so that the pump transistor is turned on to conduct the current to a source of the pump transistor;

conducting the current from the source of the pump transistor to a region of a substrate of the integrated circuit within which a protection transistor is disposed,

10 the protection transistor having a channel region of the same conductivity type as the substrate disposed between drain and source regions;

wherein the source, drain, and channel regions of the protection transistor correspond to the emitter, base, and collector of a parasitic bipolar transistor;

15 wherein the drain of the protection transistor is connected to the terminal, the source of the protection transistor is connected to a reference voltage node, and a gate of the protection transistor is connected to the gate of the pump transistor;

and wherein the step of conducting the current from the source of the pump transistor forward biases a junction between the channel and source regions of the protection transistor and causes bipolar conduction of current from the terminal to the 20 reference voltage node.

11. The method of claim 10, further comprising:

capacitively coupling current from the terminal to the gates of the pump and protection transistors via a junction capacitor.

12. The method of claim 10, further comprising:

boosting the current conducted to the region of a substrate of the integrated circuit within which a protection transistor is disposed by conducting current from the terminal to an anode of a junction diode to turn on a parasitic bipolar transistor

5 having an emitter corresponding to the anode of the junction diode, a collector corresponding to the substrate, and a base corresponding to a well within which the cathode of the junction diode is disposed.

13. An integrated circuit formed at a semiconducting surface of a substrate of a first conductivity type, comprising:

functional circuitry;

a plurality of terminals coupled to the functional circuitry;

5 at least one protection device connected to at least one of the plurality of terminals in parallel with the functional circuitry, and comprising:

a pump transistor disposed at the surface of the substrate, comprising:

10 a drain region of a second conductivity type, connected to the terminal and disposed within a well region of the second conductivity type at the surface;

a gate electrode, overlapping a portion of the well region within which the drain region is disposed, and insulated from a channel region by a gate dielectric, the channel region being of the first conductivity type; and

15 a source region, disposed at the surface adjacent to the channel region;

a protection transistor disposed at the surface of the substrate, comprising:

20 a drain region connected to the drain region of the pump transistor;

20 a source region; and  
a gate electrode connected to the gate electrode of the pump transistor and insulatively disposed over a channel region of the substrate located between the source region and the drain region; and

25 a guard ring of the first conductivity type surrounding the protection transistor, and connected to the source region of the pump transistor.

14. The integrated circuit of claim 13, wherein the drain region of the protection transistor is also disposed within a well region of the second conductivity type at the surface.

15. The integrated circuit of claim 13, wherein the at least one protection device comprises:

5 a junction capacitor, having a first plate connected to the drain regions of the pump and protection transistors and to the terminal, and having a second plate connected to the gate electrodes of the pump and protection transistors.

16. The integrated circuit of claim 13, wherein the at least one protection device comprises:

5 a junction diode, having an anode connected to the terminal and to the drain region of the pump transistor, and having a cathode connected to a power supply node.

17. The integrated circuit of claim 16, wherein the junction diode comprises:

a diffused anode region of the first conductivity type disposed within a well of the second conductivity type, and connected to the terminal and to the drain region of the pump transistor;

5                   a diffused cathode region of the second conductivity type disposed within the well of the second conductivity type, and connected to the power supply node.

18. The integrated circuit of claim 13, wherein the at least one protection device comprises:

5                   a control circuit, connected to the gates of the pump and protection transistors, and coupled to a power supply node, for biasing the gates of the pump and protection transistors to an off state responsive to the power supply node receiving a power supply voltage.

19. The integrated circuit of claim 13, wherein the protection transistor is arranged as a plurality of individual protection transistors connected in parallel;

                  wherein the pump transistor is arranged as a plurality of individual pump transistors connected in parallel;

5                   wherein the plurality of individual pump transistors and the plurality of individual protection transistors are arranged in a plurality of blocks;

                  and wherein each of the plurality of blocks is surrounded by a portion of the guard ring.

20. The integrated circuit of claim 13, wherein a first one of the plurality of terminals corresponds to a power supply terminal;

                  and wherein the at least one protection device is connected to the first one of the plurality of terminals.

21. The integrated circuit of claim 13, wherein the pump transistor has an effective channel length that is shorter than that of the protection transistor.

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